UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,902	10/30/2003	Gail A. Alverson	32475-8003US8	3055

25096	7590	11/07/2005	

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EXAMINER
IWASHKO, LEV

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/697,902	ALVERSON ET AL.
	Examiner	Art Unit
	Lev I. Iwashko	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03 November 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-19</u> is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-19</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8/15/05, 11/18/04,.</u>⅞ |16/ 04, ΙΙ/3/03

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

Information Disclosure Statement

1.   The information disclosure statement filed November 3, 2003 fails to comply with the

provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because only one of the Non Patent Literature

References was included in the application. It has been placed in the application file, but the

information referred to therein has not been considered as to the merits. Applicant is advised

that the date of any re-submission of any item of information contained in this information

disclosure statement or the submission of any missing element(s) will be the date of submission

for purposes of determining compliance with the requirements based on the time of filing the

statement, including all certification requirements for statements under 37 CFR 1.97(e). See

MPEP § 609.05(a).

Claim Rejections - 35 USC § 102

2.   The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1-19 are rejected under U.S.C. 102(b) as being anticipated by Brown et al. (US

Patent 5,542,058)

> Claim 1.   A method in a computer system of restricting access to memory, the
> method comprising: *(Abstract, lines 1-4 – State that the chip (which has a
> method) adheres to strict read and write ordering, which shows that there
> is a restriction to memory access)*
>
> -   setting a memory location to indicate a trap should occur when the
>   memory location is accessed; *(Abstract, lines 7-11 – State that the*

"specifier queue synchronization counter" is what captures (traps)
synchronization points to coordinate memory request operations)

- under control of a restricted portion of a computer program, setting a
  pointer to point to the memory location that indicates that traps to the
  pointed to memory location are enabled; *(Column 28, lines 13-15 –*
  State that there is a microtrap selector (pointer) that applies an
  address to a selector under certain conditions)

- and accessing the memory location using the set pointer so that a trap
  occurs and access to the restricted memory location is detected;
  (Column 28, lines 15-17 – State that when the microtrap occurs, the
  microcode control is transferred to the service microroutine beginning
  at the microtrap address)

- and under control of an unrestricted portion of a computer program,
  setting a pointer to point to the memory location that indicates that
  traps to the pointed to memory location are disabled; *(Column 10, lines*
  22-32 – State that there are pointers that accesses data in the register
  file in the execution unit, which houses the micropipelined unit which
  has the ability to stall and trap. Column 28, lines 44-47 – State that
  there is no microtrap from the selector, so the next address is applied
  from the selector 195 to the selector 183 for entering into the latch
  182, which means that there is a pointer to the addresses)

- and accessing the memory location using the set pointer so that a trap
  does not occur and access to the restricted memory location is allowed.
  (Column 28, lines 44-47 – State that there is no microtrap from the
  selector, so the next address is applied)

Claim 2.   The method of claim 1 wherein a user program typically accesses memory
             locations using pointers with traps enabled. *(Column 10, lines 22-32 –*
             State that there are pointers that accesses data in the register file in the
             execution unit, which houses the micropipelined unit which has the ability
             to stall and trap)

Claim 3.   The method of claim 1 including setting all memory locations of a data
             structure to indicate a trap should occur when the memory locations are
             accessed. *(Column 27, lines 53-57 – State the following: "Frequently used
             microcode is usually defined as microsubroutines stored at selected
             addresses in the control store, and when one of these subroutines is called,
             the return address is pushed onto a microstack 189 for use upon executing
             a return." In other words, all memory locations of a data structure are set
             when appropriate)*

Claim 4.   The method of claim 1 wherein when the memory location is accessed,
             invoking a trap handler. *(Column 10, lines 33-39 – State that the
             microinstruction control unit determines the next microword (memory
             location) to be fetched from the control store (memory))*

Claim 5.   A system for restricting access to memory, the system comprising: *(Figure
             1)*

             -    means for, under control of a computer program, indicating that a trap
                  should occur when a memory location is accessed; *(Column 21, lines
                  17-20 – State that the access control violation is an example of an
                  exception (which causes a trap to occur))*

             -    means for, under control of a restricted portion of the computer
                  program, setting a pointer to a memory location wherein the pointer
                  has an indication of trap handling; *(Column 21, lines 55-61 – State that
                  the microtrap causes the execution unit to inject the address (a.k.a.
                  point) for the event into the address latch for the control store)*

             -    means for accessing the memory location; and *(Column 22, lines 45-
                  49 – Describe how memory is accessed)*

             -    means for handling a trap wherein propriety of the access is detected.
                  *(Column 21, lines 60-61 – Declares that the "execution unit 23
                  microcode routine will process the exception as appropriate")*

Claim 6.   The system of claim 5 wherein the indication of trap handling is enabled.
             (Column 27, lines 34-36 – State that there is a selector that selects
             whether or not the microtrap is enabled)

Claim 7.   The system of claim 5 wherein the indication of trap handling is disabled.
             (Column 27, lines 34-36 – State that there is a selector that selects
             whether or not the microtrap is enabled)

Claim 8.   The method of claim 5 wherein the propriety is unauthorized. *(Column 2,*
             lines 5-8 – State that "the PC returned is the PC of the opcode of the next
             instruction to execute. The microcode then constructs the appropriate
             exception frame on the stack, and dispatches to the operating system
             through an appropriate vector ")

Claim 9.   The method of claim 5 wherein the propriety is authorized. *(Column 2,*
             lines 5-8 – State that "the PC returned is the PC of the opcode of the next
             instruction to execute. The microcode then constructs the appropriate
             exception frame on the stack, and dispatches to the operating system
             through an appropriate vector ")

Claim 10.   A computer-readable medium for restricting access to memory,
             comprising: *(Figure 1)*

             -   a data structure with a plurality of elements; *(Figure 7 – Shows a data*
                 structure with a plurality of elements)

             -   a pointer to an element in the data structure, *(Column 28, lines 13-15 –*
                 State that a microtrap selector (pointer) has a number of inputs and
                 applies an address to a selector)

             -   the pointer having an indication of whether a trap is enabled depending
                 on whether a restricted or unrestricted portion of a computer program
                 is accessing the data structure; *(Column 28, lines 13-15 – State that*
                 there is a microtrap selector (pointer) that applies an address to a
                 selector under certain conditions)

             -   for each element, an indication of whether a trap is enabled; *(Column*
                 10, lines 22-32 – State that there are pointers that accesses data in the

register file in the execution unit, which houses the micropipelined unit which has the ability to stall and trap)

- and a handler including instructions for handling the enabled trap. *(Column 10, lines 33-39 – State that the microinstruction control unit determines the next microword (memory location) to be fetched from the control store (memory))*

Claim 11.   The computer-readable medium of claim 10 wherein the indication for an element is enabled. *(Column 10, lines 22-32 – State that there are pointers that accesses data in the register file in the execution unit, which houses the micropipelined unit which has the ability to stall and trap)*

Claim 12.   The computer-readable medium of claim 10 wherein the handler is invoked when the element in the data structure is accessed through a pointer whose indication is enabled. *(Column 10, lines 33-39 – State that the microinstruction control unit determines the next microword (memory location) to be fetched from the control store (memory). Column 28, lines 13-15 – State that there is a microtrap selector (pointer) that applies an address to a selector under certain conditions)*

Claim 13.   The computer-readable medium of claim 10 wherein the handler is not invoked when the element in the data structure is accessed through a pointer whose indication is disabled. *(Column 28, lines 44-47 – State that there is no microtrap from the selector, so the next address is applied from the selector 195 to the selector 183 for entering into the latch 182, which means that there is a pointer to the addresses)*

Claim 14.   The computer-readable medium of claim 13 wherein the indication for an element is disabled. *(Column 28, lines 44-47 – State that there is no microtrap (element is disabled) from the selector, so the next address is applied)*

Claim 15.   The computer-readable medium of claim 13 wherein the handler is invoked when the element in the data structure is accessed through a pointer whose indication is enabled. *(Column 10, lines 33-39 – State that*

the microinstruction control unit determines the next microword (memory

location) to be fetched from the control store (memory). Column 28, lines

13-15 – State that there is a microtrap selector (pointer) that applies an

address to a selector under certain conditions)

Claim 16.　　　A system for restricting access to memory comprising: *(Figure 1)*

- a component that sets a memory location to indicate a trap should

  occur when the memory location is accessed; *(Abstract, lines 7-11 –*

  State that the "specifier queue synchronization counter" is what

  captures (traps) synchronization points to coordinate memory request

  operations)

- a component that, under control of a restricted portion of a computer

  program, sets a pointer to point to the memory location that indicates

  that traps to the pointed to memory location are enabled; *(Column 28,*

  lines 13-15 – State that there is a microtrap selector (pointer) that

  applies an address to a selector under certain conditions)

- and accesses the memory location using the set pointer so that a trap

  occurs and access to the restricted memory location is detected;

  (Column 28, lines 15-17 – State that when the microtrap occurs, the

  microcode control is transferred to the service microroutine beginning

  at the microtrap address)

- and a component that, under control of an unrestricted portion of a

  computer program, sets a pointer to point to the memory location that

  indicates that traps to the pointed to memory location are disabled;

  (Column 10, lines 22-32 – State that there are pointers that accesses

  data in the register file in the execution unit, which houses the

  micropipelined unit which has the ability to stall and trap. Column 28,

  lines 44-47 – State that there is no microtrap from the selector, so the

  next address is applied from the selector 195 to the selector 183 for

  entering into the latch 182, which means that there is a pointer to the
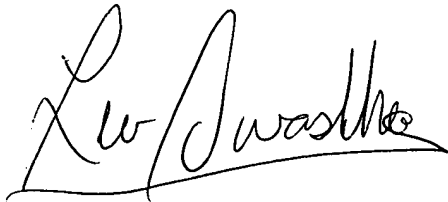
  addresses)

- and accesses the memory location using the set pointer so that a trap does not occur and access to the restricted memory location is allowed. *(Column 28, lines 44-47 – State that there is no microtrap from the selector, so the next address is applied)*

Claim 17.   The system of claim 16 wherein a user program typically accesses memory locations using pointers with traps enabled. *(Column 10, lines 22-32 – State that there are pointers that accesses data in the register file in the execution unit, which houses the micropipelined unit which has the ability to stall and trap)*

Claim 18.   The system of claim 16 including a component that sets all memory locations of a data structure to indicate a trap should occur when the memory locations are accessed. *(Column 27, lines 53-57 – State the following: "Frequently used microcode is usually defined as microsubroutines stored at selected addresses in the control store, and when one of these subroutines is called, the return address is pushed onto a microstack 189 for use upon executing a return." In other words, all memory locations of a data structure are set when appropriate)*

Claim 19.   The system of claim 16 wherein when the memory location is accessed, a trap handler is invoked. *(Column 10, lines 33-39 – State that the microinstruction control unit determines the next microword (memory location) to be fetched from the control store (memory))*
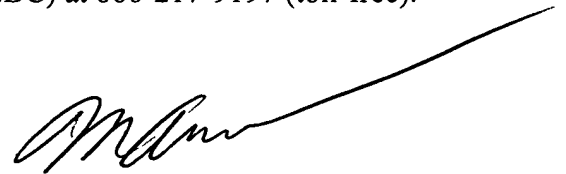
Conclusion

4.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for

unpublished applications is available through Private PAIR only. For more information about

the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the

Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER